Electronic Version

Stylesheet Version v1.1.1

Clock Presence Detector Comparing Differential Clock to Common-Mode Voltage

Abstract

Presence or absence of a differential clock is detected. The voltage of each differential clock line is compared to the common-mode voltage and integrated over time by a capacitor. The capacitor is discharged during the portions of the clock cycle that the differential line is over the common-mode voltage. If the clock stops pulsing the capacitor is charged by a current source to activate a clock-loss signal. The clock-loss detector is ideal for high-frequency operation since each differential clock line is applied to only one transistor gate. The common-mode voltage generates a bias voltage for a differential amplifier that receives the true and complement differential clock lines. Diodes prevent capacitor charging by reverse current flow from the differential amplifier when the clock is inactive. The averaged peak voltage or envelope of the differential input signals is detected.